11'A

Notice of Allowability	Application No.	Applicant(s)	
	10/692,606	STEINHOFF, ROBERT M.	
	Examiner	Art Unit	
	Cuong Q. Nguyen	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☐ This communication is responsive to _____.

2. ☒ The allowed claim(s) is/are *1-12 and 22*.

3. ☒ The drawings filed on *24 October 2004* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

CUONG NGUYEN
PRIMARY EXAMINER

AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

1. (Original) A semiconductor device comprising:

a voltage node coupled to a first p-type region;

a first n-type region having a first side adjoining the first p-type region;

a second p-type region having a first side adjoining a second side of the first n-type region;

a second n-type region having a first side adjoining a second side of the second p-type region;

a clamping circuit intercoupled between the second n-type region and ground; and

a switching circuit intercoupled between the second p-type region and ground.

2. (Original) The device of claim 1, further comprising a resistive element intercoupled between the first n-type region and the voltage node.

3. (Original) The device of claim 2, wherein the resistive element comprises a resistor.

4. (Original) The device of claim 1, wherein the voltage node comprises a bond pad.

5. (Original) The device of claim 1, wherein the switching circuit comprises a resistor.

6. (Original) The device of claim 1, wherein the switching circuit comprises a transistor.

7. (Original) The device of claim 6, wherein the transistor comprises an NPN transistor.

8. (Original) The device of claim 6, wherein the transistor comprises an NMOS transistor.

9. (Original) The device of claim 1, wherein the clamping circuit comprises a transistor.

10. (Original) The device of claim 9, wherein the transistor comprises an NPN transistor.

11. (Original) The device of claim 9, wherein the transistor comprises an NMOS transistor.

12. (Original) The device of claim 1, wherein the clamping circuit comprises a diode.

13. (Withdrawn) A method of providing a semiconductor device utilizing a silicon controlled rectifier, the method comprising the steps of:

providing a semiconductor device having a silicon controlled rectifier formed therein;

providing a clamping structure, coupled to the silicon-controlled rectifier, adapted to prevent a p-n junction within the silicon controlled rectifier from retaining a forward bias;

providing a switching structure, coupled to the p-type portion of the p-n junction and adapted to ground the p-type portion during normal operation of the semiconductor device.

14. (Withdrawn) The method of claim 13, wherein the step of providing the switching structure comprises providing a resistor.

15. (Withdrawn) The method of claim 13, wherein the step of providing the switching structure comprises providing a transistor.

16. (Withdrawn) The method of claim 15, wherein the step of providing the transistor further comprises providing an NPN transistor.

17. (Withdrawn) The method of claim 15, wherein the step of providing the transistor further comprises providing an NMOS transistor.

18. (Withdrawn) The method of claim 13, wherein the step of providing the clamping structure comprises providing a diode.

19. (Withdrawn) The method of claim 13, wherein the step of providing the clamping structure comprises providing a transistor.

20. (Withdrawn) The method of claim 19, wherein the step of providing the transistor further comprises providing an NPN transistor.

21. (Withdrawn) The method of claim 19, wherein the step of providing the transistor further comprises providing an NMOS transistor.

22. (Original) A system for providing a electrostatic discharge protection in a semiconductor device, utilizing a silicon controlled rectifier, the system comprising:

a silicon controlled rectifier having a first p-type region coupled to a voltage node, a first n-type region having a first side adjoining the first p-type region, a second p-type region having a first side adjoining a second side of the first n-type region, and a second n-type region having a first side adjoining a second side of the second p-type region;

a clamping structure, intercoupled between the second n-type region and ground, and adapted to prevent the junction between the second p-type region and the second n-type region from retaining a forward bias ; and

a switching structure, intercoupled between the second p-type region and ground, and adapted to ground the second p-type region during normal operation of the semiconductor device.